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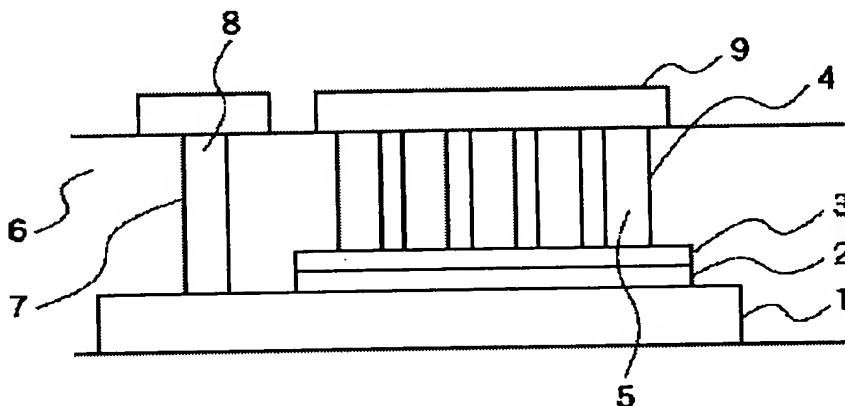
(54) SEMICONDUCTOR DEVICE
AND ITS MANUFACTURING
METHOD

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a construction of an MIM capacitor which is suitable for a fine wiring process, has small parasitic resistance and parasitic capacitance and has a high capacitance.

SOLUTION: This semiconductor device has a 1st electrode 1 which is formed on a semiconductor substrate and has a flat plane shape as a whole, a dielectric layer 2 which is formed on the 1st electrode and has a flat plane shape as a whole, a 2nd electrode 3 which is formed on the dielectric layer 2 and has a flat plane shape as a whole, an interlayer insulating layer 6 which covers the 1st and 2nd electrodes and the dielectric layer as a whole and has a plurality of via-holes 4 and 7 bottomed by the surface of the 2nd electrode 3 therein, and conductive layers filling the via-holes.

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公 告

登 録

名 称 半導体装置およびその製造方法

抄 録【要約】 (修正有)【課題】 微細配線加工に適した、寄生抵抗、寄生容量の少ない、高容量値を有するMIM型コンデンサの構造を提供する。【解決手段】 本発明の半導体装置は、半導体基板上に形成され、その全体が一平面形状を有する第1の電極1と、前記第1の電極の上面に形成され、その全体が一平面形状を有する誘電体層2と、前記誘電体層の上面に形成され、その全体が一平面形状を有する第2の電極3と、前記第1、第2の電極、および前記誘電体層全体を被覆し、前記第2の電極表面を底面とする複数のビアホール4、7を内部に具有する層間絶縁層6と、前記ビアホールを充填する導電層とを具備する。

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